

### **REMARKS**

This amendment is a full and timely response to the Final Office Action dated March 16, 2009. Claims 1 – 6 are pending in the above identified application, with claims 1, 3, and 5 being independent. In this amendment, claims 1, 3, and 5 have been amended. Support for these amendments is variously found in the Applicant's specification as filed, including but not necessarily limited to paragraph [0050] – [0053] of the specification as represented in U.S. Pub. No. 2006/0152461 A1. Reconsideration and allowance is requested in view of the following remarks. *No new matter has been added by these amendments.*

Claims 1, 3, and 5 have been rejected under 35 U.S.C. § 112 as allegedly being indefinite for failing to point out and distinctly claim the subject matter of which Applicant regards as the invention. This rejection is respectfully traversed.

Claim 1 has been amended to remove and replace the indefinite language, and thus, the rejection is now moot. Claims 3 and 5 have been similarly amended.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 1, 3, and 5 under 35 U.S.C. § 112.

Claims 1 – 2 and 5 – 6 have been rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by *Edwards*, U.S. Patent Number 6,498,438 (*Edwards*). This rejection is respectfully traversed.

Independent claim 1 recites “[a] *method for operating a constant current circuit, comprising:*

*after connecting a sampling capacitor connected between a gate and a source of a first transistor and a drain of the first transistor to a reference current source and setting a voltage across the sampling capacitor to a voltage between the gate and the source produced while the first transistor is driven by a reference current of the reference current source,*

*cutting off the connection among the sampling capacitor, the first transistor and the reference current source, as well as connecting the drain of the first transistor to a driving target, and driving the driving target by a current of the first transistor due to the voltage between the gate and the source that is set in the sampling capacitor,*

*wherein said cutting off the connection comprises applying a first signal to a gate of a second transistor connected between the drain of the first transistor and the reference current source,*

*a second signal that is a logical inverse of said first signal to a gate of a third transistor connected between the gate and drain of the first transistor, and*

*a third signal to a gate of a fourth transistor connected between the drain of the first transistor and the driving target.”*

*Edwards* fails to disclose or suggest these claimed features. *Edwards* discloses a driver circuit that uses a single input word for switching transistors to produce an output current. *Edwards* specifically uses a single sample line to turn transistors T2 and T3 on and off thereby forcing both transistors T2 and T3 to be in the same logic state as dictated by the sample line. (*Edwards*, col. 9 line 2).

In contrast to *Edwards*, Applicant’s claimed invention applies separate first, second, and third signals in order to connect and cut off the constant current circuit to the reference current and the driving target. In this regard, each transistor may be triggered in different stages or at different time intervals, rather than always keeping transistors T2 and T3 in the same logic state as is done in *Edwards*.

Further and by way of example, the timing signal xNcnt1 is held at an L level when the timing signals Ncnt2 is held at an H level; the respective logical values of the timing signals xNcnt1 and Ncnt2 are simultaneously switched; and “the respective timing signals xNcnt1, Nact and Ncnt2 are supplied so that the constant current circuit 26 operates . . . to function as a constant current circuit. (U.S. Publication 2006/0152461 A1, Specification ¶¶ [0050] - [0053]).

Consistent with these distinctions, *Edwards* does not disclose or suggest “*a third signal to a gate of a fourth transistor connected between the drain of the first transistor and the driving target.*”

Because *Edwards* fails to disclose, teach, or suggest various features of claim 1, a *prima facie* anticipation rejection has not been established, and withdrawal of this rejection is respectfully requested. See, e.g., *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) (“A claim is anticipated only if each and every element as set forth in

the claim is found, either expressly or inherently described, in a single prior art reference”). See also *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1566 (Fed. Cir. 1989). (“The identical invention must be shown in as complete detail as is contained in the ... claim.”).

For reasons similar to those provided for claim 1, independent claim 5 is also neither disclosed by *Edwards*. The dependent claims are also distinct for their incorporation of the features respectively recited in the independent claims as well as for their own, separately recited patentably distinct features.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 1 – 2 and 5 – 6 under 35 U.S.C. § 102(b) as being anticipated by *Edwards*.

Claims 3 and 4 have been rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over *Edwards* and *Yamazaki*, U.S. Publication No. 2006/0267899 (*Yamazaki*). This rejection is respectfully traversed at least for the following reasons.

Independent claim 3 recites, “[a] *flat display device constructed so that a display section made of pixels arranged in a matrix form, a vertical driving circuit for sequentially selecting the pixels of the display section through gate lines, and a horizontal driving circuit for driving pixels selected through the gate lines, by signal lines of the display section,*

*characterized in that:*

*the horizontal driving circuit comprises:*

*a digital-to-analog conversion circuit for performing digital-to-analog conversion processing of gradation data indicative of gradations of the pixels; and*

*a buffer circuit for driving the signal lines by means of an output signal from the digital-to-analog conversion circuit;*

*the buffer circuit drives the signal lines by a source follower circuit formed by connecting a constant current circuit to a source of a transistor; and*

*the constant current circuit is configured such that, after connecting a sampling capacitor connected between a gate and a source of a first transistor and a drain of the first transistor to a reference current source and setting a voltage across the sampling capacitor to a voltage between the gate and the source produced while the first transistor is driven by a reference current of the*

*reference current source, cuts off the connection among the sampling capacitor, the first transistor and the reference current source, as well as connects the drain of the first transistor to a driving target and drives the driving target by a current of the first transistor due to the first voltage between the gate and the source that is set in the sampling capacitor;*

*a first signal applied to a gate of a second transistor having a gate, a source, and a drain, connected between the drain of the first transistor and the reference current source;*

*a second signal that is a logical inverse of said first signal to a gate of a third transistor connected between the gate and drain of the first transistor, and*

*a third signal to a gate of a fourth transistor connected between the drain of the first transistor and the driving target.”*

Similarly to the discussion above, these claimed features are not disclosed or suggested by *Edwards*.

Further, *Edwards* does not disclose “a digital-to-analog conversion circuit for performing digital-to-analog conversion processing of gradation data indicative of gradations of the pixels; and a buffer circuit for driving the signal lines by means of an output signal from the digital-to-analog conversion circuit; the buffer circuit drives the signal lines by a source follower circuit formed by connecting a constant current circuit to a source of a transistor,” which the Office Action admits. (Office Action Page 7).

Thus, *Edwards* does not disclose nor in any way suggest the Applicant’s claimed features of independent claim 3. *Yamazaki* does not remedy the deficiencies of *Edwards*.

*Yamazaki* discloses an LCD display that is said to avoid deterioration of the image due to image persistence. *Yamazaki* is relied upon for purported disclosure of a digital to analog conversion circuit, a buffer circuit, and their related features conceded to be absent from *Edwards*. However, *Yamazaki* offers no disclosure or suggestion of the above-described features that are also absent from *Edwards*.

Accordingly, since even a combination of *Edwards* and *Yamazaki* would still fail to yield features of Applicant’s claimed invention, a prima facie case of obviousness for independent claim 3 has not been presented.

In view of the above amendment, applicant believes the pending application is in condition for allowance. If any further issues remain, the Examiner is invited to telephone the undersigned to resolve them.

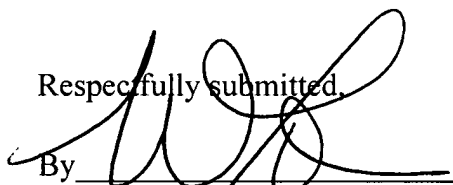
Please treat any concurrent or future reply, requiring a petition for an extension of time under 37 C.F.R. §1.136, as incorporating a petition for extension of time for the appropriate length of time.

This response is believed to be a complete response to the Office Action. However, Applicant reserves the right to set forth further arguments supporting the patentability of their claims, including the separate patentability of the dependent claims not explicitly addressed herein, in future papers. Further, for any instances in which the Examiner took Official Notice in the Office Action, Applicant expressly does not acquiesce to the taking of Official Notice, and respectfully requests that the Examiner provide an affidavit to support the Official Notice taken in the next Office Action, as required by 37 CFR 1.104(d)(2) and MPEP § 2144.03.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 18-0013, under Order No. SON-3660 from which the undersigned is authorized to draw.

Dated: May 17, 2010

Respectfully submitted,



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